The camera of the ASTRI SST-2M prototype for the Cherenkov Telescope Array

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ABSTRACT

In the context of the Cherenkov Telescope Array observatory project, the ASTRI SST-2M end-to-end prototype telescope, entirely supported by the Italian National Institute of Astrophysics, is designed to detect cosmic primary gamma ray energies from few TeV up to hundreds of TeV. The ASTRI SST-2M prototype camera is part of the challenging synergy of novel optical design, camera sensors, front-end electronics and telescope structure design. The camera is devoted to imaging and recording the Cherenkov images of air showers induced by primary particles into the Earth's atmosphere. In order to match the energy range mentioned above, the camera must be able to trigger events within a few tens of nanoseconds with high detection efficiency. This is obtained by combining silicon photo-multiplier sensors and suitable front-end electronics. Due to the characteristic imprint of the Cherenkov image that is a function of the shower core distance, the signal dynamic range of the pixels and consequently of the front-end electronics must span three orders of magnitude (1:1000 photo-electrons). These and many other features of the ASTRI SST-2M prototype camera will be reported in this contribution together with a complete overview of the mechanical and thermodynamic camera system.

Keywords: Imaging Atmospheric Cherenkov Telescope, CTA, gamma-rays, ASTRI, telescope prototype, camera sensors and electronics, dual mirror

1. INTRODUCTION

The ASTRI ("Astrofisica con Specchi a Tecnologia Replicante Italiana") is a flagship project funded by the Italian Ministry of Education, University and Research and led by the Italian National Institute of Astrophysics (INAF). The project foresees the realization of an end-to-end prototype telescope of small-size class, according to the Cherenkov Telescope Array (CTA)[1] scientific requirements. The ASTRI small-size telescope in a dual-mirror configuration (SST-2M) is intended for the investigation of primary gamma rays of energy ranging from a few TeV up to 100 TeV[2]. The ASTRI SST-2M telescope prototype adopts a focal plane camera based on an array of monolithic multi-pixel Silicon Photo-Multiplier (SiPM) sensors that, coupled with a specifically designed front-end electronics and a dual mirror optics configuration, represents an innovative solution for the detection of Atmospheric Cherenkov light[3]. The camera of the ASTRI prototype telescope is designed to catch and record the Cherenkov light pulses during the night, in the wavelength interval of 300-700 nm, produced by charged particles in the Air Shower cascade process initiated and sustained by the primary particles entering the Earth's atmosphere. The Cherenkov photons, conveyed by the dual mirror

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optics to the camera, are detected by means of SiPM sensors and converted to appropriate digital signals closely representative of the Air Shower Cherenkov image. This image will appear almost instantaneously on the focal surface camera (FSC), exhibiting a local maximum intensity surrounded by less intense signals fading gradually away. The shower images on the camera last from few ns to tens of ns and must be promptly identified against the unavoidable Night Sky Background (NSB) light and detector dark noise. Figure 1 shows a simulated gamma ray event on the FSC together with NSB light and detector dark noise. The Cherenkov image is actually buried inside the incoherent background (NSB + detector dark noise) and its identification depends strongly on several telescope and camera parameters that need to be taken into account and optimized in order to obtain the required performance. Starting from the definition of the scientific objectives (an iterative process with the CTA science team), technical solutions for mechanics, electronics, calibration and thermal control have been studied, analyzed and realized to satisfy system and scientific requirements. The identification of critical elements and analysis of expected performance is currently in progress in order to finalize the trade-off processes and consolidate the design through subsystem feasibility. The design criteria, when applicable, comply with the SST-CTA (Small Size Telescope - Cherenkov Telescope Array) requirements and pursue the objective of achieving design quality and reliability.

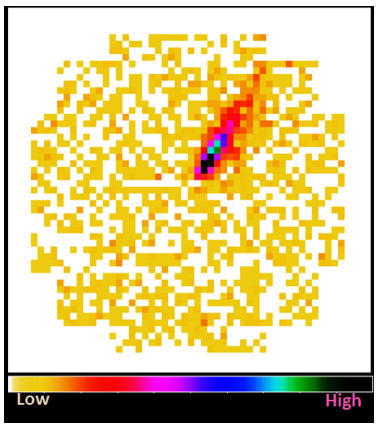

Figure 1. Image from the ASTRI SST-2M camera of an on-axis simulated gamma-ray event. The primary gamma-ray signal had an energy of 10 TeV and a core distance of 142.77 m. The night sky background is at a level of 1.9×10^{12} ph m^{-2} s^{-1} sr^{-1}. The color bar shows the number of photoelectrons per pixel.

2. CAMERA

The camera is controlled and operated by dedicated and customized software/firmware. It is composed of four hardware main block assemblies, as shown in Figure 2:

- Mechanical
- Power Supply
- Electronics
- Thermal System

The Mechanical Assembly has the main function of containing the entire camera electronics, including power distribution system, cooling/heating thermoelectric system, fiber-optic calibration system and ancillary devices. It provides the mechanical interface to the telescope structure. The lid, the Poly-Methyl MethAcrylate (PMMA) protective window and the Photo Detection Modules (PDMs) support structure are also included.

The Power Supply Assembly has the main function of generating and distributing the required voltages among the various electronics components, from a 24 V single power supply.

The Electronics Assembly comprises SiPMs, Front-End Electronics (FEE), Back-End Electronics (BEE) and the ancillary electronics. The main function of FFE is to convert the analog SiPM signals in digital signals while the BEE controls and manages the overall system, including data management formats, Lid mechanisms and fiber-optic calibration tool by means of a dual core Advanced RISC Machine (ARM) processor embedded in a ZYNQ -7000 FPGA[4]

(Field Programmable Gate Array). The BEE provides also the functions needed to process and transmit the images as converted by the FEE.

The Thermal System provides thermal management, control and monitoring of the camera temperature that has to be kept at a fixed known value during telescope observations.

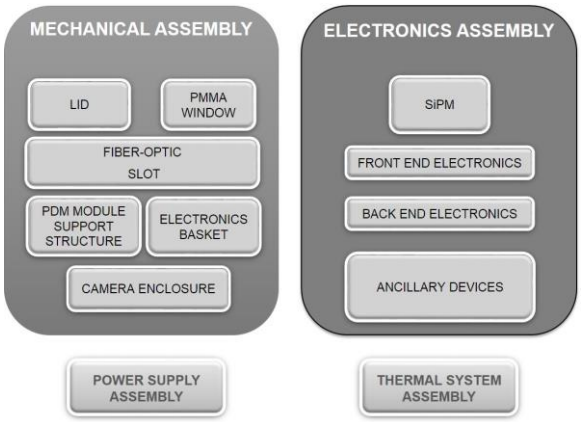

Figure 2. Camera functional blocks representation.

3. MECHANICAL ASSEMBLY

The camera mechanical assembly includes several components detailed below and it is usually referred to as the "camera body". The camera body is, by definition, from a point of view of mechanical design, the complete deliverable object containing the controls, the detectors, the internal image processor, the thermal system and the associated circuitry. Moreover, the camera body includes the interface to the mechanical structure of the telescope. The global mechanical design of the camera body takes into account all these elements and, according to the requirements, estimates the center of gravity, weight and moments of inertia for the resulting camera geometry. The local reference system of the camera body has its origin in the hypothetical opto-mechanical center of the "entrance surface" of the central PDM. An exploded 3D visualization of the mechanical design is shown in Figure 3 together with the full-size mock-up of the camera. The camera dimensions are 500 mm, 490 mm, 560 mm respectively (bottom diameter, height, top diameter) for a total weight of 50 kg. A detailed description of the parts constituting the mechanical assembly is given below.

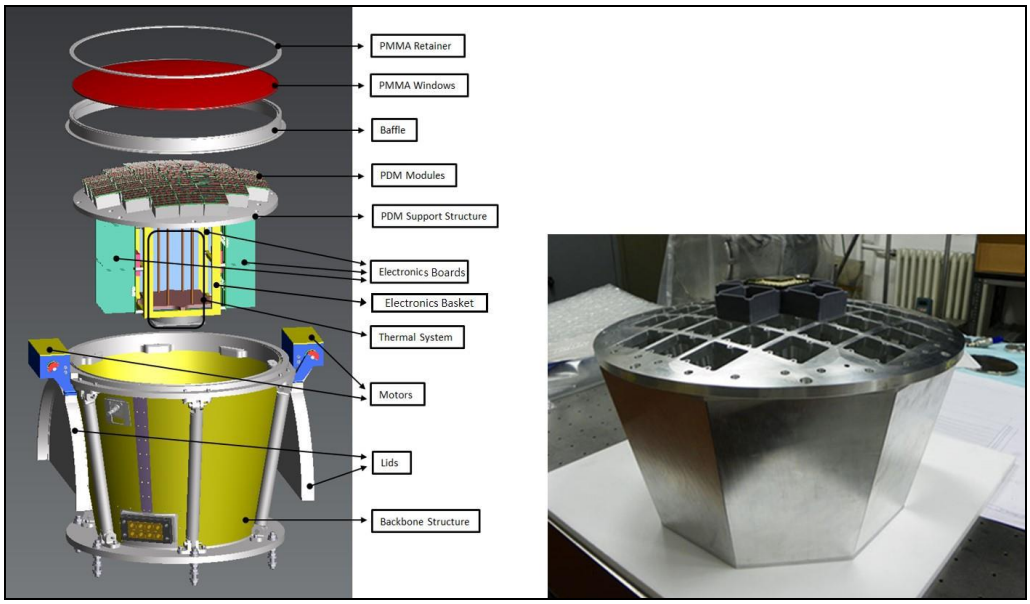

Figure 3. Exploded view of the Camera body assembly (left) and full-size mock-up (right).

3.1 LID

The camera is equipped with light-tight lids in order to prevent accidental incidence of sunlight on the focal surface detectors, which could be catastrophic in case of direct light reflected by the mirrors and to perform simultaneous detector relative calibration even during day light. The lid is composed by two "petals", mounted on a dedicated support. The two petals are conceived to perform 270 degrees rotation from the closed position by means of two stepper motors mounted as shown in Figure 4. A description of electro-mechanical components of the lids is given in paragraph 7.4.

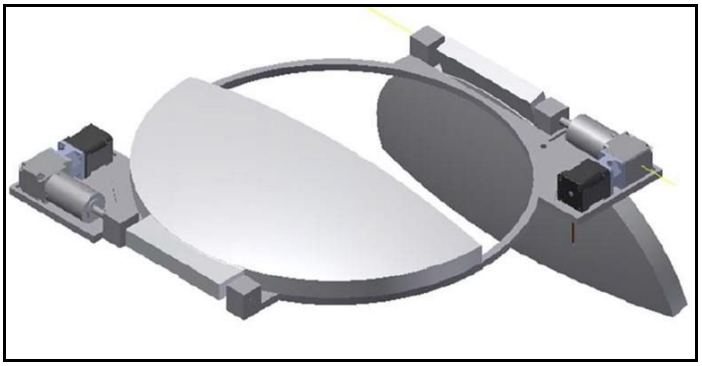

Figure 4. Lid and servomotors disposition.

3.2 PMMA window

An optical transparent PMMA window prevents sand and dust from being deposited on the PDMs and keeps a stable temperature environment around the focal plane which is needed to avoid gain variations of the SiPMs. The window is mounted on the backbone PDM support structure. The PMMA window is modeled with the same radius of curvature as the focal surface. The thickness of the window is 3 mm with a diameter of 501 mm. As shown in Figure 5, along the border of the backbone plate flange of the PDM support structure a groove is designed to accommodate a 1.2 mm optical fiber. This optical fiber, in optical contact with the PMMA window, allows the photons generated by continuous or pulsed LED light to illuminate the PMMA window almost uniformly. The Fiber-PMMA window set up is used for monitoring the SiPM pixels relative gain and efficiency variations.

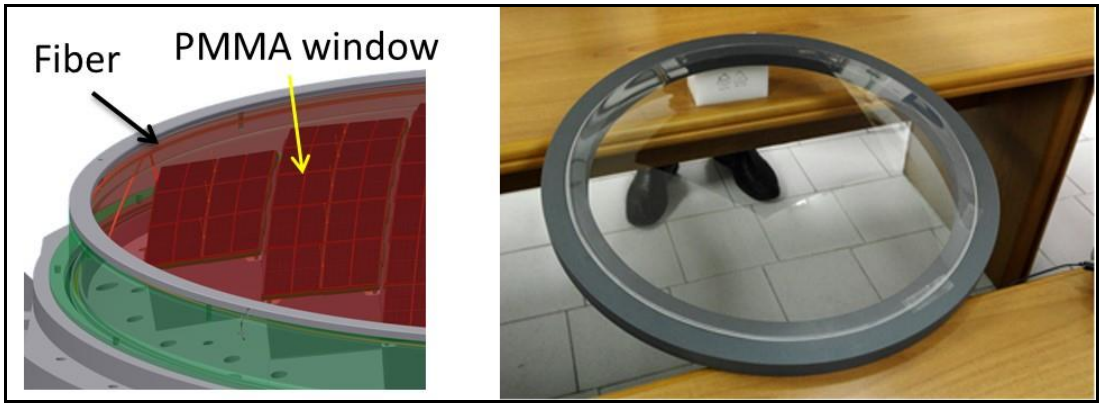

Figure 5. Side emission optical fiber slot machined out in the backbone plate flange (left). PMMA window and backbone flange mock-up picture (right).

3.3 PDM unit

The PDM is the mechanical unit containing the SiPMs board, FEE and ARTIX 7 FPGA Printed Circuit Boards (PCBs). Each PDM module is mechanically interfaced to the PDM support structure through three bolts screwed from the bottom side of it. PCBs are connected to the PDM modules by means of four through screws. Figure 6 shows the exploded view of the PDM and the machined aluminum case.

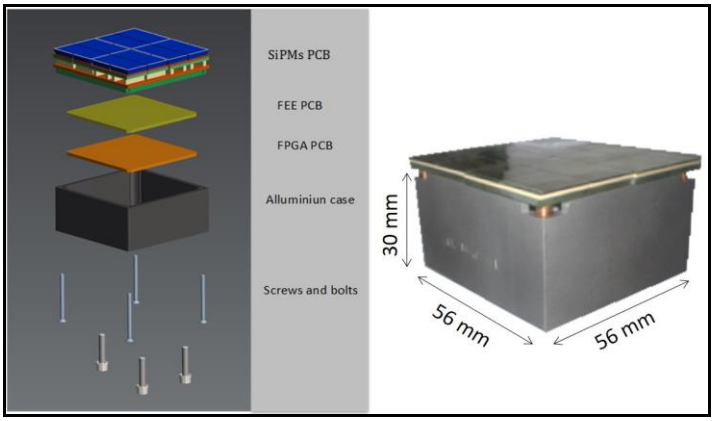

Figure 6. PDM exploded view (left). PDM aluminum case with SiPM PCB mounted on top (right).

3.4 PDM support structure

The PDM support structure is composed by a spherically-shaped mounting interfaced to the electronics basket and to the backbone structure. This structure is machined out of standard flat plates of Al Si1MgMn (EN AW-6082). Efficient thermal management is obtained by embedding heating pipes into the PDM support structure. For the best thermal contact, the heating pipes are bent and soldered into the metallic support. The spherically-shaped mounting hosts all 37 PDM modules forming the focal surface and two CCD cameras devoted to monitor some optical features (see Sect.7.1). The electronics basket structure is screwed to the bottom of the backbone flange plate. A 3D representation of the spherical shape mounting and the machined mock-up are shown in Figure 7.

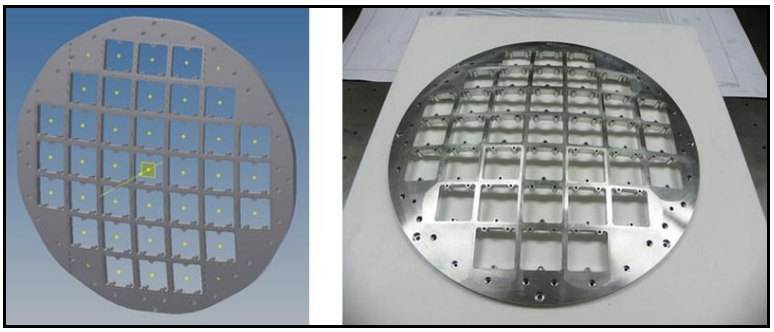

Figure 7. PDM 3D mechanical support (left). The machined mock-up (right).

3.5 Electronics basket

The electronics basket is composed of a bottom plate and four joints; it contains the PCBs. Inside the electronics basket are the PCBs containing the BEE and the Voltage Distribution Board. The thermoelectric module is attached to the bottom plate.

3.6 Camera enclosure

The camera enclosure, as shown in Figure 8, is made of two separate parts: the thermal enclosure and the backbone structure.

The thermal enclosure is designed to host the electronics basket and the Peltier-based thermal system screwed on the bottom. This structure is in thermal contact with the PDM support structure by means of heat pipes and is thermally isolated from the backbone structure by wrapping it in a synthetic flexible sheet.

The backbone structure consists of two circular flanges - upper and bottom - machined out of a standard flat aluminum plate (EN AW-6082), and jointed together via standard circular tube made by BOSCH®.

The bottom plate (disc shape) is machined in order to permit "the feed through" of the electronic cables.

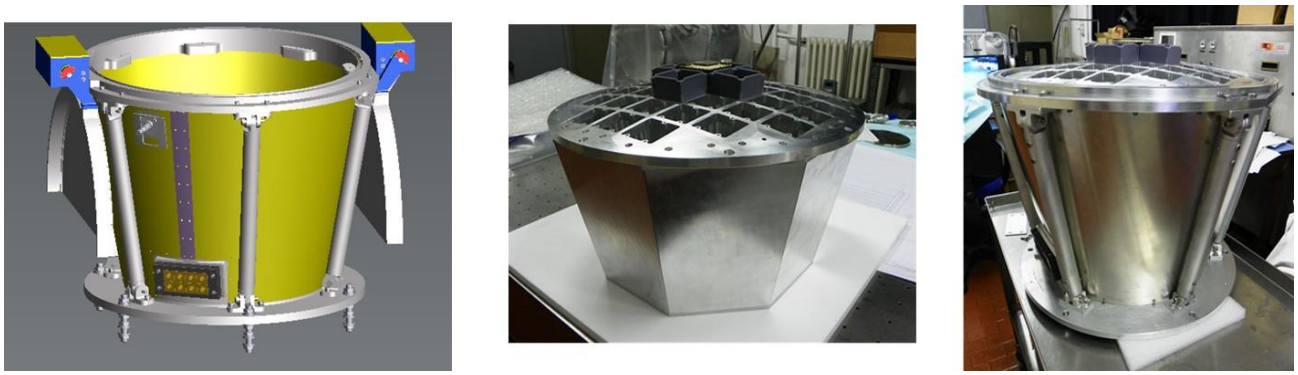

Figure 8. 3D representation of the backbone structure (left) and the related machined mock-up (center and right).

4. POWER SUPPLY ASSEMBLY

The Power Supply Assembly provides the required power regulation to the system. All the voltages needed for the electronic devices, as defined in the Electronics Assembly, are provided by a Voltage Distribution Board (VDB) that consists of a main board and 37 daughter boards. Figure 9 shows the functional block diagrams of the main and daughter board respectively. The VDB converts one low-voltage supply (24 V) input to individually protected output voltages. This unit provides several regulated outputs to fulfill the system requirements. The VDB consists of power conditioning electronics based on DC/DC converters. The VDB provides power to the drivers of the Lid motors and to the entire Electronic Assembly. Housekeeping functions as voltage or current are available for monitoring of the VDB status. The unit implements overload and overvoltage protection circuitries in order to avoid failure propagation.

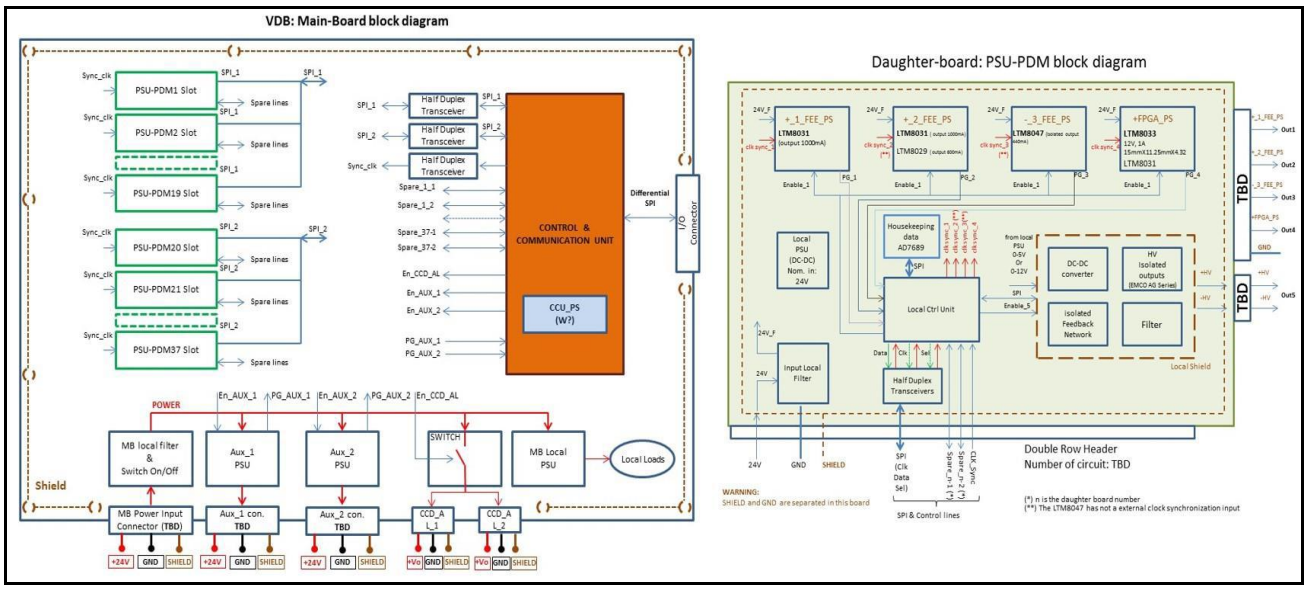

Figure 9. Functional block diagrams of the main board and of one of the daughter boards constituting the VDB.

5. ELECTRONICS ASSEMBLY

The electronics assembly includes the focal surface electronics constituted by SiPMs, FEE and BEE where communication serial lines are implemented for controlling the ancillary devices including Fiber Optic Calibration (FOC) tool, GPS and the pointing CCD cameras.

For a more comprehensive understanding of the ASTRI camera architecture it is necessary to introduce, in a descriptive way, the schematic of the focal surface camera layout. The baseline focal surface layout (FOV=9.6°) consists of 37 PDMs. The top of each PDM consists of a layer of 4×4 SiPM units (Hamamatsu S11828-3344M), each of which consists of a monolithic SiPM of 4×4 pixels with pixel size of 3 mm × 3 mm. A "logical" pixel corresponding to a channel is made up by electrically-grouping 2×2 pixels with a resulting size of 6.2 mm × 6.2 mm. A pictorial scheme of the focal surface arrangement is shown in Figure 10. Each SiPM unit has four channels and each PDM has 64 channels. In total 1984 channels are needed to convey the information, represented by photoelectron pulse signals coming from the FSC SiPM sensors. The PDMs' modularity, both mechanical and electrical, assures flexibility in maintenance and inspection, making the replacement of faulty PDMs in any position of the FSC easy.

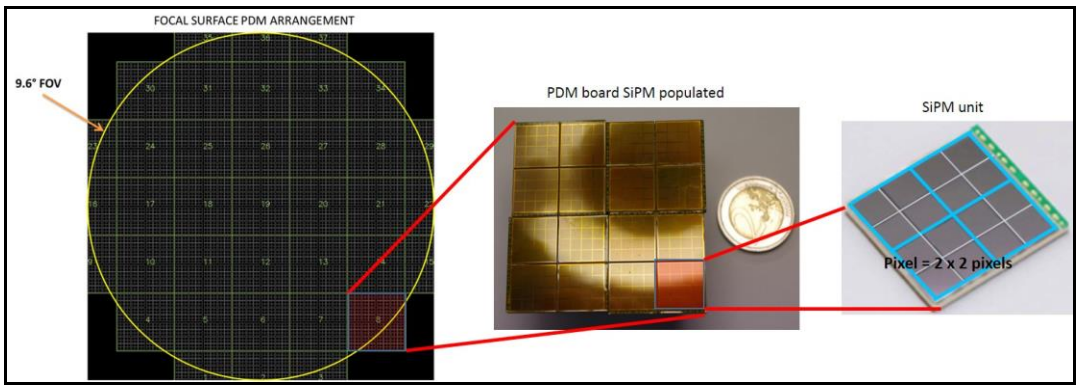

Figure 100. Focal surface layout. The diameter of the yellow circle corresponds to a FOV of 9.6°. PDM SiPM board and SiPM unit are also shown.

In the FSC mechanical layout, the electronics of the focal surface exhibits modularity at the PDM level. Moreover, each PDM works independently from the others making it possible to replicate the electronics, giving clear benefits regarding debugging, harness complexity and manufacturing costs.

The electronics hosted in the PDM, basically, is responsible for the acquisition and the processing of SiPM pulses in a manner that complies with pre-defined and unvarying specification, making them usable by the BEE. The most critical part of the PDM electronics is the analog FEE that must preserve the information contained in the signal pulses for further measurements such as energy and pixel time tagging. The proximity electronics (the FEE) consists of two (32 channels each) CITIROC[5] (Cherenkov Image Telescope Integrated Read Out Chip) ASIC (Application-Specific Integrated Circuit) supported by an ARTIX 7 FPGA that controls operations such as the CITIROC registers, reading-out of digitalized data and trigger signal management. Each FPGA has also the duty of performing the trigger algorithms.

The BEE has the role of concentrating, distributing, synchronizing and transmitting scientific data, ancillary data, housekeeping (HK) and controls from/to the PDMs and an external system (workstation-console) in which quick-look, monitoring functions and data archiving are implemented. In the BEE the software for the telescope "scientific" and "engineering" operational mode as well as the camera calibration procedures are also implemented. All these operations and functions are supplied by a ZYNQ-7000 FPGA that is the heart of the BEE. The communication between the FEE and the BEE is substantially handled by fast serial lines with the exception of few dedicated parallel lines between the FEE and the BEE. Two Ethernet lines provide the communication between BEE and workstation-console.

The voltage distribution board provides the regulated voltages needed to the SiPMs, FEE and BEE.

5.1 PDM Front-End Electronics

PDM front-end electronics comprises the SiPM PCB, the CITIROC PCB and the ARTIX 7 FPGA PCB. The PCBs are accommodated in the PDM aluminum case as shown in Figure 11. The PCBs are tight together in order to minimize space and optimize the heat exchange between them.

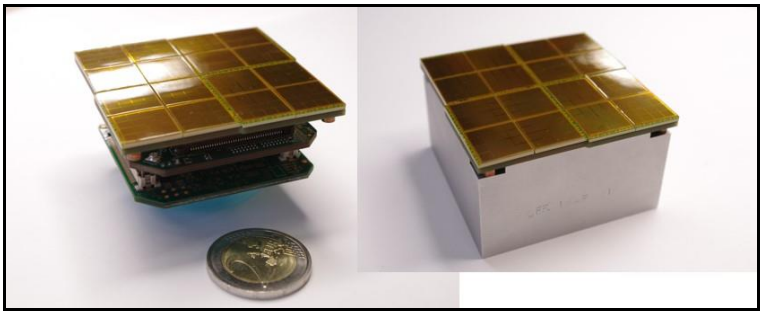

Figure 111. PDM Front End PCBs accommodated in the PDM aluminum case.

5.2 SiPM Unit and SiPM PCB

Figure 12 illustrates the mechanical dimensions of a Hamamatsu S11828-3344M SiPM. This SiPM is a new type of photon-counting device made up of multiple APD (Avalanche Photo Diode) cells of 50 μm size operated in Geiger mode. The SiPM is essentially an opto-semiconductor device with excellent photon-counting capability and the advantages of low voltage operation and insensitivity to magnetic fields. As shown in the picture, the SiPM is a monolithic device with pixels of 3 mm × 3 mm set out to form an array of 4×4 pixels. This geometry allows multiple devices to be arranged in a buttable format.

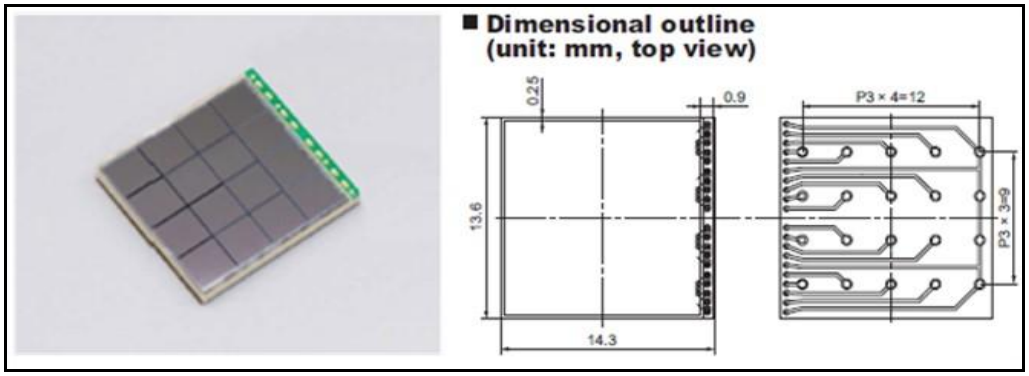

Figure 12. SiPM unit (left) and dimensions of the device (right).

The PDM SiPM PCB is formed of four SiPM units. Each SiPM device is soldered to the PCB using a ball grid array soldering technique. At the bottom of the PCB there are soldered 9 precision analog temperature sensors (LM94023), with another one soldered on the center of the top side of the PCB. These sensors are used for SiPMs temperature monitoring. A photograph of the completed PCB is shown in Figure 13.

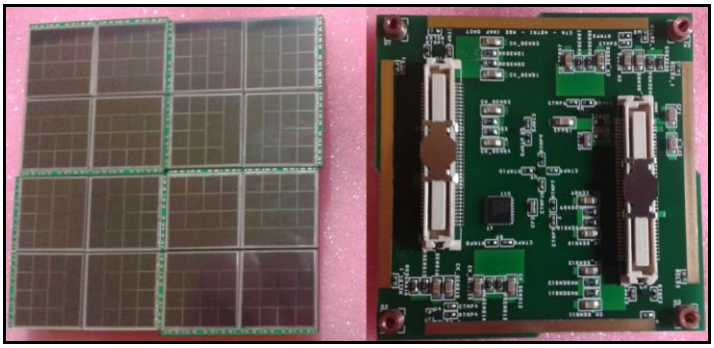

Figure 13. PDM SiPM PCB top side (left) and bottom side (right).

5.3 CITIROC PCB

The FEE is designed to acquire electrical signals from the SiPMs, typically a short current pulse, tailor the time response (i.e. "shape" the output pulse) of the system to optimize the minimum detectable signal and make it available for subsequent signal processing. The base line FEE is based on the CITIROC chip and two dual channel 14-bit ADCs that convert low-gain and high-gain sampled values to digital outputs. The CITIROC chip integrates:

- 32-channel front-end readout
- Individual 8-bit DAC for SiPM gain adjustment
- Common 10-bit DAC + 4-bit DAC/channel for threshold adjustment
- 32 high-gain + 32 low-gain programmable gain preamplifiers
- 2 multiplexed analog outputs (high-gain, low-gain)
- 32 trigger outputs

with a total power consumption of 200 mW/chip (6.25 mW/channel). Figure 14 shows the block diagram of the FEE and its related PCB.

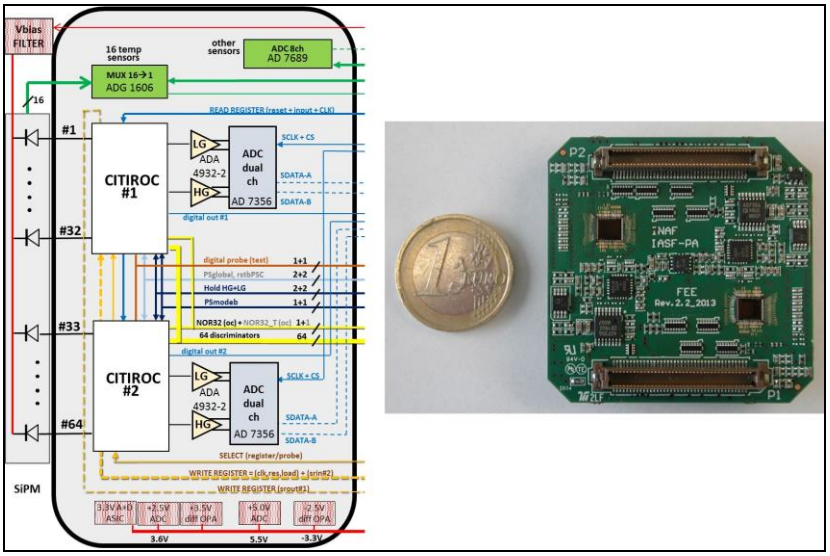

Figure 14. Block diagram and PCB of the CITIROC front-end.

In order to process the 64 PDM pixels two CITIROC ASICs are connected in a daisy chain. Each ASIC is configured to undertake the desired functions by loading the configuration registers serially (slow control mode). This operation is managed by the ARTIX 7 FPGA[6] under the control of the BEE. The slow control performs several functions, including:

- SiPM gain adjustment, varying the SiPM applied operating voltage through an 8-bit programmable DAC (one per channel).
- Setting of gain for the high-gain and the low-gain preamplifier and shaper chain (programmable from 1 to 15 for low gain and from 10 to 150 for high gain)
- Setting of the shaper time for the high-gain and the low-gain chain respectively (programmable from 12.5 ns to 100 ns with step of 12.5 ns).
- Setting of discriminator threshold by means of programmable 10-bit DAC (for 32 channels) and 4-bit DAC (one per channel).
- Setting of the mode of operation: Sampling and Hold or Peak Detector.

Sampled values, as required by the trigger setting, are converted to digital signals by means of two dual 14-bit ADCs and serially transferred to the ARTIX 7 FPGA that is in charge of this operation. Thanks to the two, parallel, AC coupled voltage preamplifiers per channel, read out of the charge from 160 fC to 320 pC (ie. 1 to 2000 photoelectrons with SiPM Gain = 10^6, with a photoelectron to noise ratio of 10) is achievable.

5.4 ARTIX 7 FPGA PCB

The ARTIX 7 FPGA governs and controls all the operations of the PDM front-end. It is interfaced to the BEE through a bidirectional serial line and to the CITIROC PCB via a serial line and a few dedicated digital lines. It receives commands from the BEE and sends data and HK information to the BEE. Figure 15 shows the block diagram of the board (based on ARTIX 7 FPGA) and a picture of the PCB.

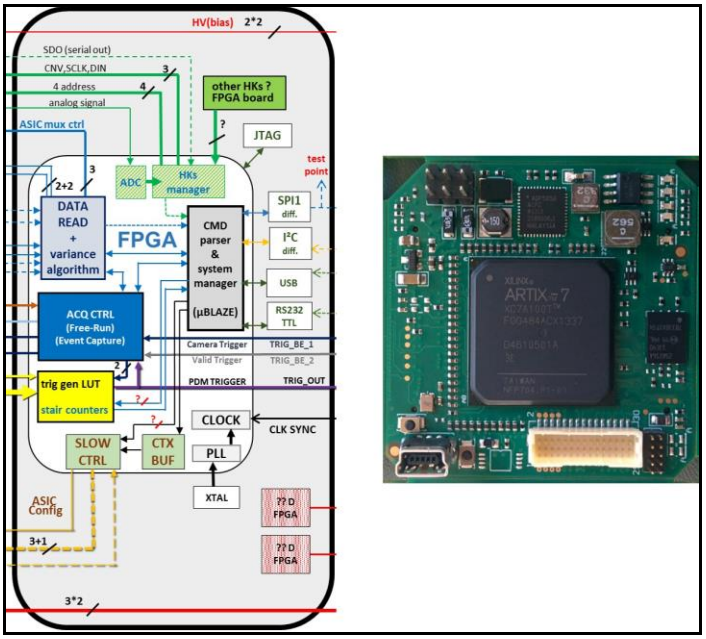

Figure 15. Block diagram and PCB of the ARTIX 7 FPGA front-end.

The trigger algorithm is implemented in the ARTIX as well as other algorithms needed for the acquisition and processing of the signals and in particular the management of the following functions:

- I/O interface to ASIC PCB.
- I/O interface to BEE.
- Custom application procedures (trigger generation, data acquisition, ASIC configuration).
- Implementation of custom algorithms.
- R/W of allocated Registers and Memory Buffers on chip.

The ARTIX 7 FPGA PCB hardware includes all the devices such as the oscillator, voltage regulators and filters needed for the correct operation of the FPGA. The PCB hosts an oscillator to allow stand-alone operations, while for time synchronization reasons, a master clock input is available for keeping every PDM on time.

5.5 Back End Electronics PCB

The BEE is hosted on a separate common board. The design of the BEE is based on the powerful FPGA, ZYNQ-7000, which manages the communication to/from the FEE and the external world. The back-end FPGA is the heart of the electronics, since it is in charge of the complete data and command management of the instrument, interfacing the detectors to the external world. It lies between the PDM front-end electronics and the Camera Server and Camera Controller System. It is the primary component of the real-time scientific data processing capability (the processing pipeline) of the ASTRI SST-2M Telescope. Its primary responsibility is to perform basic data assembly, formatting and processing services and to support the procedure desired for real-time inspection of the camera data stream.

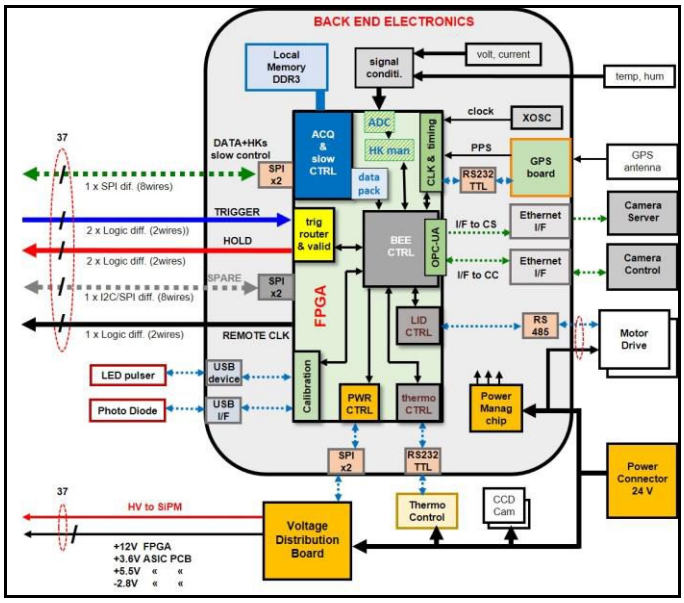

Figure 16. Simplified block diagram of the BEE.

The major functions the BEE must perform are:

- Receive commands from the Camera Controller and perform the related procedures.
- Receive data from the front-end in real-time.
- Deliver suitably formatted results to the Camera Server System.
- Perform a limited number of additional processes upon user request.

The simplified high-level block diagram of the BEE is illustrated in Figure 16.

The back-end will be responsible for the data handling and the generation of basic data assembling, formatting and delivery as well as other related processing activities. It is designed and implemented as a real-time data processing system capable of consuming and processing data and operating at a rate greater than or equal to the rate generated by the trigger of the telescope (600 Hz).

The back-end will also sit alongside the Camera Control System that will provide all the external commands and controls to the BEE and will receive all errors, warning, performance and other reports from the back-end.

6. THERMAL SYSTEM ASSEMBLY

The camera is thermally controlled through a thermoelectric system based on a Peltier cell manufactured by UWE Electronics[7] . It is able to dissipate the 200 W power produced by the camera electronics. The thermal system is a direct-

to-air thermoelectric assembly that uses impingement flow to transfer heat. It offers dependable, compact performance by cooling/heating the camera via an "ad hoc" heating pipes network. Heat is absorbed through a cold plate and dissipated though a high-density heat exchanger equipped with an air ducted shroud and fan. The heat pumping action is generated by the thermoelectric and achieves a high coefficient of performance to minimize power consumption. The thermal system performs the operations required to assure a proper working temperature of the camera electronics (from 15°C to 20°C, approximately) and in particular to maintain the SiPMs at a constant temperature. The system makes use of a bi-directional thermostatic controller that can operate in both heating and cooling modes and provide temperature control and system functions, including separate fan control, low voltage protection, and alarm. The RS232 interface enables parameters to be read and controlled, as well as providing for real-time function setting. A photograph of the direct-to-air thermoelectric assembly and of the bi-directional thermostatic controller is shown in Figure 17.

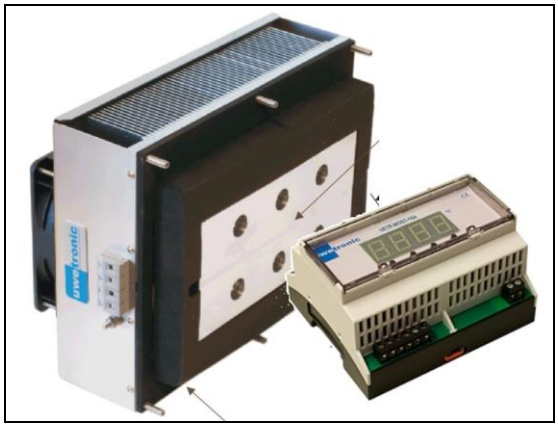

Figure 17. The Direct-to-Air Thermoelectric Assembly (left) and the bi-directional Thermostatic Controller (right).

7. ANCILLARY ELECTRONICS DEVICES

Ancillary electronic devices are used to provide additional functions for camera operation. They are located inside the camera and interfaced to the BEE.

7.1 CCD cameras

Two small CCD cameras (size 45 mm) will be installed on the PDM support structure, near its edges, to monitor the primary mirror flexures. A minimum of two cameras is necessary to ensure all the panels of the primary mirror are covered. The output of the control system will be the centroid of each laser spot corresponding to each panel in the field of view of the small CCDs. These centroids, evaluated in relation to the reference position corresponding to the no-flexure situation of the telescope, permits the differential pointing of the telescope with respect to the values of the encoders to be obtained. In this way, the required accuracy will be reached (12 arcsec rms on the sky post-calibration).

7.2 FOC

The relative gain calibration of the camera is based on a new illumination technique[8]. Relative calibration of SiPMs' gain is accomplished using a fiber-optic positioned around the backbone plate flange. The fiber is in contact with the border of the PMMA window and acts as a driving medium for the light diffused by the optical fiber. Light pulses, programmable in intensity and duration, are conveyed to one of the open extremities of the fiber-optic by means of a multi-color LED hosted in a box which also contains the electric circuitry and is controlled by a dedicated output from the BEE-FPGA. The light enters the PMMA and undergoes a series of total internal reflections and scattering processes, before exiting the window on the front side, skyward, or on the backside, illuminating the PDM units. By tuning the intensity of the light emitted by the optical fiber it is possible to achieve a suitable illumination level to calibrate the PDMs. LED light pulses are managed by the PicoLAS PLCS-21[9] control unit connected with a LDP-V 03-100 UF3 driver module. The PLCS-21 control unit allows full control of pulse width, pulse current and repetition rate provided by the LDP-V 03-100 UF3 driver module. This unit provides a galvanically isolated USB interface as well as an RS232 port. Light intensity emitted by the other extremity of the optical fiber is read by a silicon photodiode, S150C, connected to a PM100USB - USB Power and Energy Meter Interface Unit (Thorlabs) that allows energy measurement and control

of stability of the LED. The power head is spectrally calibrated over the whole wavelength operating range and detects light from nanoWatts up to 5 mW.

7.3 GPS Synchronization

A compact and lightweight GPS receiver, M12M GPS[10], is used for time synchronization and provides time-tagging for triggered events. Standard features include precise one-pulse-per-second (1pps) outputs. The BEE provides the required 10 ns precision processing, with a proper circuit embedded in the FPGA part, the 1pps.

7.4 Lids

Opening and closing of the telescope lids are performed by means of two motor controllers SMCI12 by Nanotec[11], mounted in the motor box, located outside the camera. The stepper motor controller SMCI12 is an extremely compact and cost-effective constant-current power output stage with integrated closed loop current control. The controller is RS485-connected to the ZYNQ-7000 board and managed by the on-board OPC-UA server.

8. CAMERA SOFTWARE AND FIRMWARE

Figure 18 shows the camera architecture in terms of the hardware and software blocks responsible for the monitoring and control of the camera where only the significant hardware modules involved in the interactions are reported.

The hardware subsystems have been described in previous paragraphs; for completeness two external components that have an important role in the overall camera architecture should be defined, the Control Client and the Camera Server.

- The Control Client is represented by a personal computer where the high-level slow-control software is executed. This client represents the entry point for the final user (engineer or operator) who interacts with the camera using Graphical User Interfaces (GUI) in order to access monitoring and control functionality.
- The Camera Server represents the Data Acquisition (DAQ) Workstation responsible for receiving and storing the different data packets (Housekeeping, Calibration and Scientific) produced by the camera.

At the software level, two main classes of components are defined: Slow and Fast.

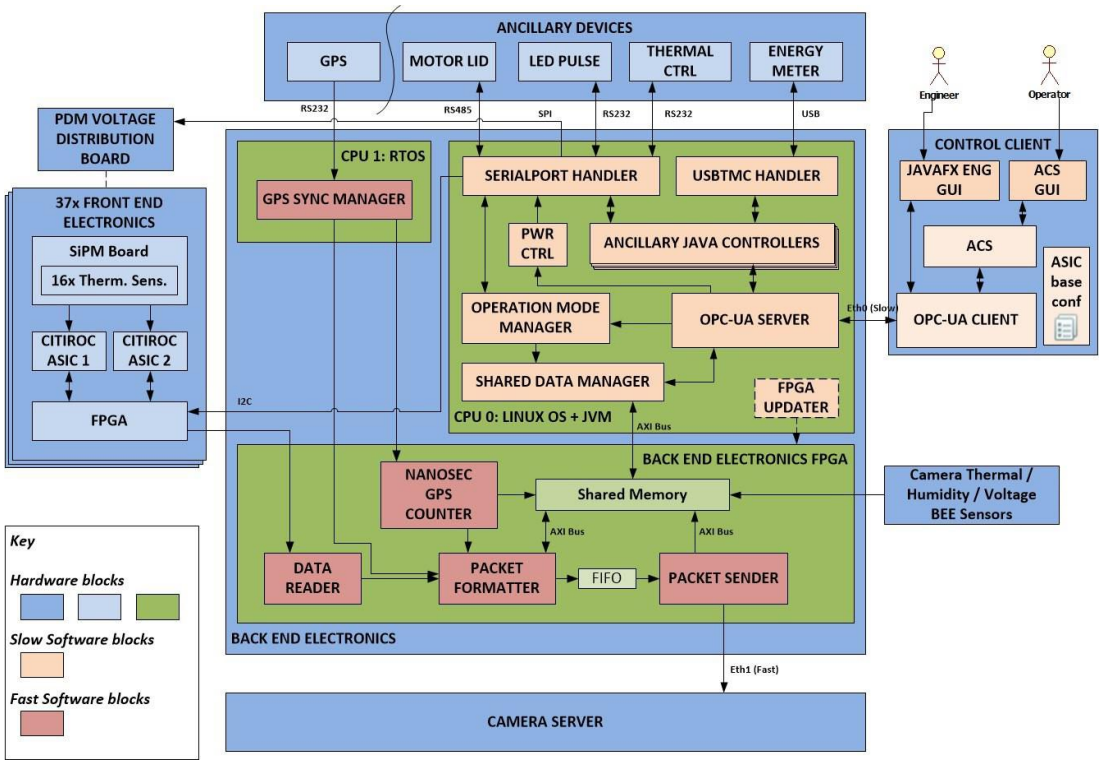

Figure 18. The block diagram of the software/firmware camera architecture.

8.1 Slow Software Components

Slow software components are developed in the Control Client and in one of the ARM processors of the BEE which has a Linux and Java Runtime environment installed on it. Most of the code is written in Java, except for some code in C for physical channel and memory management.

To facilitate the information exchange between Control Client and the BEE and to manage commands and controls for the camera processes, the platform-independent standard OPC UA[12] has been adopted. This standard allows various kinds of systems and devices to communicate by sending messages between Clients and Servers over various types of networks. In brief, an OPC UA Server integrates data, alarms and events defining an address space which contains the physical quantities to be observed and controlled, defining appropriate nodes that can be queried by OPC UA Clients.

Every user interaction with the GUI of the Control Client has a corresponding OPC UA command that is dispatched from the client to the server in the BEE. This interconnection is made through the Ethernet channel in charge of the slow control communication. Once a command is received by the OPC UA Server, it calls the related software components that implement the desired functionality.

Components related to the ancillary devices are the Ancillary Java Controllers. They query and set values of the devices sending and receiving strings through the related physical channel using the Serial Port Handler or the USBTMC Handler. String commands are related to the particular hardware chosen for the devices. Usually they are a subset of all commands described in the various software specification manuals, according to the physical quantities to be observed and controlled as defined in the address space of the OPC UA Server.

The Power Control (PWR CTRL) component is similar to the ancillary controllers. It controls the power of the FEEs sending commands to the PDM VDB through a Serial Peripheral Interface (SPI) using the Serial Port Handler.

The Operation Mode Manager is a complex component that manages the overall state of the camera. It is called when a command such as “start acquisition in scientific mode with these parameters” arrives at the OPC UA Server and manages all the operations needed to accomplish that task. Typical operations are, for example, sending the configurations for the ASICS to the FEE, iteratively modifying the configurations according to the elapsed time or changes in environmental variables (i.e. temperatures) and sending relevant data to the programmable logic subsystem of the BEE.

The programmable logic and Linux environments of the BEE are in fact physically decoupled, as are the processes running within them. In order to create a method of communication to exchange data between these two parts, a specific memory mapped region has been defined inside the programmable logic part of the BEE. This shared memory is accessed through an Advanced eXtensible Interface (AXI) Bus and contains the data in a prefixed and well defined table. In particular, it contains all the data provided by the Linux environment to the programmable logic as the complete information relating to packets to format and sent to Camera Server, as well as all the information provided by programmable logic to the Linux environment in order to monitor variables like the temperatures of the SiPMs, voltages and other housekeeping data. At the logic level this shared table is realized as device file accessed for reading and writing operations by the Shared Data Manager.

FPGA Updater Module is responsible for the update of the code deployed in the programmable logic environment; it performs, via remote access, the operations required for maintenance.

8.2 Fast Software Components

Fast software components do not implement particularly complex business logic because they are responsible for simple tasks that require high speed in their execution and for this reason they are realized inside the ARM-system with the Real Time Operating System (RTOS) and in the programmable logic side of the BEE.

Main functionalities provided by these components are:

- Management of GPS current time with real time precision (GPS Sync Manager module)
- Acquisition of data from the FEE units (Data Reader module)
- Packing data in dedicated packets format (Packet Formatter module)
- Sending packets to Camera Server (Packet Sender module)
- Management of GPS current time with 10 nanoseconds precision (Nanosec Gps Counter module)

9. CONCLUSIONS

The ASTRI SST-2M camera is part of the end-to-end prototype telescope currently under construction. The technological solutions adopted for the camera comply with the CTA requirements and include all the necessary hardware, software and firmware to perform Cherenkov gamma-ray observations. The ASTRI SST-2M telescope will be installed in Italy at the INAF "M.C. Fracastoro" station (1735 m a.s.l) located in Serra La Nave[13] during Fall 2014. The camera will be installed in early 2015 and the whole integrated system will go through the scientific validation phase.

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REFERENCES

[1] Acharya, B.S., et al., "Introducing the CTA concept," Astroparticle Physics 43, 3–18 (2013).
[2] Pareschi, G., et al., "The dual-mirror Small Size Telescope for the Cherenkov Telescope Array," Proc. 33rd ICRC, ArXiv:1307.4962 (2013).
[3] Catalano, O., e al., "The ASTRI SST-2M Prototype: Camera and Electronics," Proc. 33rd ICRC, ArXiv: 1307.5142 (2013)
[4] XILINX, "Zynq-7000 Silicon Devices," http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/silicon-devices/index.htm
[5] Fleury, J., et al., "Petiroc and Citiroc: front-end ASICs for SiPM read-out and ToF applications," JINST 9 C01049 (2014)
[6] XILINX, "ARTIX," http://www.xilinx.com/products/silicon-devices/fpga/artix-7/
[7] UWE Electronic, "UETR-MOST-16° Thermoelectric Controller datasheet," http://www.uweelectronic.de/images/datenblaetter_temp/regler/datasheet_uetr-most-16a.pdf
[8] Rodeghiero, G, Catalano, O., Segreto, A. et al., "Illumination Technique for the Relative Calibration of the ASTRI SST-2M Camera, " NIM-A, Nuclear Instrum. & Methods - Section A, in press (2014)
[9] PicoLAS Schulz Electronic GmbH, "PLCS-21 user guide," http://www.schulz-electronic.de/out/media/PLCS-21_B_E.pdf
[10] I-Lotus Pte. Ltd., "GPS Products M12 Timing Receiver datasheet'" http://www.ilotus.com.sg/~ilotus/sites/all/themes/zeropoint/pdf/m12m/M12M%20-%20User%20Guide%20(Ver%201.0.0).pdf
[11] Nanotec, "SMCI12 Stepper Controller technical manual," http://en.nanotec.com/fileadmin/files/Handbuecher/Motorcontrols/SMCI12_Technical-Manual_V1.2.pdf
[12] OPC Unified Architecture, "Specification, Part 1: Overview and Concepts, Release 1.02, July 10, 2012," https://opcfoundation.org/developer-tools/specifications-unified-architecture/part-1-overview-and-concepts
[13] Maccarone, M.C., Leto, G., Bruno, P., Fiorini, M., Grillo, A., Segreto, A., Stringhetti, L., "The Site of the ASTRI SST-2M Telescope Prototype, " Proc. 33rd ICRC, ArXiv: 1307.5139 (2013).