PSPICE HIGH-LEVEL MODEL AND SIMULATIONS OF THE EASIROC ANALOG FRONT-END

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Abstract

The present paper is intended to implement and simulate the Extended Analogue Silicon-photomultiplier Integrated Read-Out Chip (EASIROC) fully analogue front-end model, in order to investigate its foremost characteristics and demonstrate its practical effectiveness when its analogue inputs are driven by the silicon photomultiplier (SiPM) signals. The circuit models of all functional blocks are described. Frequency and dynamic features of all circuit front-end sections are briefly addressed, and design mathematical equations are derived as well. PSPICE simulations of each single model are carried out to analyse and confirm its analogue behaviour.

Key Words

Analogue circuits, front-end model, PSPICE simulations, silicon photomultipliers

1. Introduction

EASIROC (Extended Analogue Silicon-photomultiplier Integrated Read-Out Chip) is a chip produced by OMEGA and proposed as front-end of the camera at the focal plane of ASTRI, a flagship project of the Italian Ministry of Education, University and Research, which is aimed to build a prototype for the small size telescopes of the Cherenkov telescope array (CTA) [1]. The focal plane of the ASTRI prototype [2]–[8] is based on silicon photo-multiplier (SiPM) sensors [9]–[14], and requires *ad hoc* front-end electronics able to catch the fast pulses of Cherenkov light.

The ASTRI telescope will be characterized by innovative technological solutions in terms of mirror structure, focal plane sensors and front-end electronics. For the first time in Cherenkov telescopes design, the ASTRI prototype will be equipped with a dual-mirror Schwarzschild–Couder optical system arranged in a compact layout configuration, allowing the exploitation of a compact low-cost, lightweight and low-power consumption camera [15], [16].

EASIROC is a 32-channel fully analogue front-end dedicated to the gain trimming and read-out of SiPMs. For each channel, two parallel AC-coupled voltage pre-amplifiers ensure the read-out of the pulse charge. Two tuneable slow-shapers are adopted to reduce the noise components amplitude out of a specific pre-determined frequency range. A trigger line is available from the high gain pre-amplifier. It is composed of a 15 ns peaking time fast-shaper followed by a discriminator circuit providing the signal trigger [17]–[20].

The availability of an electrical model of the EASIROC analogue core is important for a detailed understanding and a reliable interpretation of the physical interactions between SiPMs and conditioning electronics. On the basis of this model, reliable circuit-level simulations can be performed on the SiPM detector coupled to the front-end electronics. In addition, a simulated front-end model may also be profitably exploited for choosing the optimal front-end architecture for the particular application requirements before executing experimental measurements on the real chip.

The present article is devoted to the implementation and simulation of the fully analogue model of the EASIROC chip, designated as front-end at the focal plane of the ASTRI Cherenkov telescope, in order to promote additional understanding of the specific signal conditioning electronics for the optical sensors of the ASTRI camera, and confirm its theoretical effectiveness in driving the output signals of the SiPM detectors.

2. Analogue Front-End Model

The entire simulated analogue front-end is illustrated in Fig. 1. It basically consists of an SiPM matrix model for the generation of the input pulses, a pre-amplifier section including two adjustable capacitive-feedback amplifiers modulating the pulse voltage amplitude in accordance

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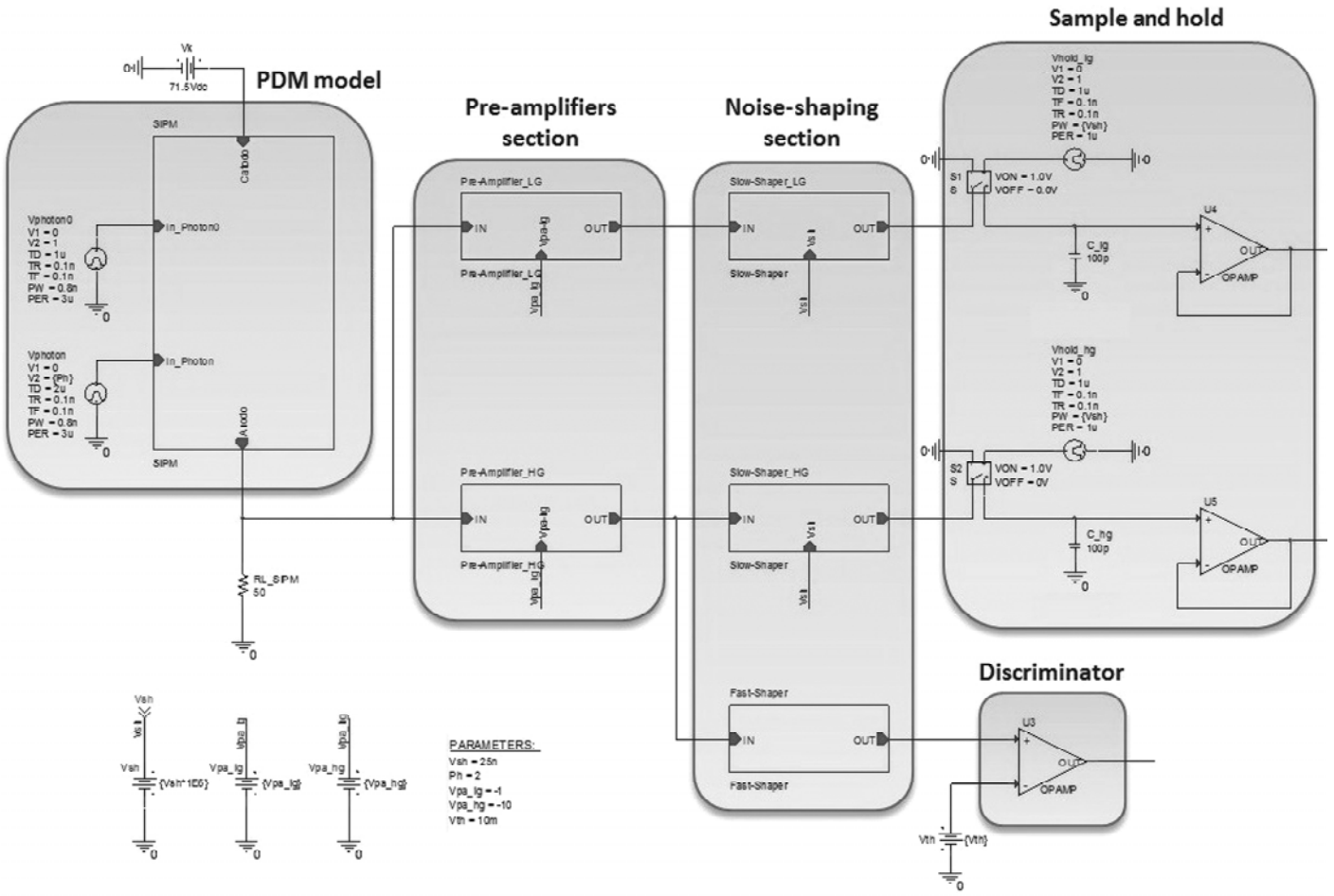

Figure 1. Analogue EASIROC front-end circuit schematic model used for simulations.

with particular sensitivity requirements, a noise-shaping section for noise reduction composed of a bipolar fast-shaper and two tuneable shaping time slow-shapers, a fast single-threshold discriminator for the trigger signal generation and an analogue sample-and-hold memory for digital data acquisition.

The SiPM matrix model in Fig. 1 produces output current pulses in accordance with proper voltage-step inputs applied to a series of voltage-controlled switches with specific thresholds. Such current signals flow through a 50-Ω load resistor and generate the output voltage pulses related to the number of photons detected by the SiPM matrix.

The programmable parameters by means of which the realized front-end model can control the analogue signal processing of the input detectors, act upon:

- the number of input photons detected by the SiPM matrix;
- the closed-loop gain magnitude of the low-gain and high-gain pre-amplifiers;
- the shaping time of both low-gain and high-gain slow-shapers;
- the reference threshold of the discriminator.

Also, the voltage-controlled switches enabling the two sample-and-hold cells in both low-gain and high-gain channel branches are synchronized with the shaping times of the relevant slow-shapers, to provide correct data acquisition.

3. PDM Electrical Model

The basic ASTRI camera element is referred to as the photon detection module (PDM) and will host the SiPM detectors matrix in a 4×4 square array. To build a PDM, each detector unit is mounted on a small PCB of equal dimensions, in the back side of which two connectors and a temperature sensor for gain adjustment are soldered, so that all detectors can be coupled, side by side, onto a bigger hosting board to create a complete structural module, as shown in Fig. 2.

The electrical SiPM model in [21], [22] is employed on the basis of the behaviour of each single microcell of the detector structure, in order to simulate the discharge of N_f cells over a total number N_{tot} of microcells.

The output voltage pulses of the 4×4 input SiPM matrix of the ASTRI camera simulated by the adopted electrical model when closed to a 50-Ω load resistor R_L is characterized by the following features:

- rise time constant $\tau_{rise} \approx 1\,\text{ns}$;
- fall time constant $\tau_{fall} \approx 50\,\text{ns}$;
- peak voltage amplitude per photon $V_{peak} \approx 100\,\mu\text{V}$.

The output-generated pulse signals feed the EASIROC single-channel input, and are then processed by the subsequent sections of the front-end model.

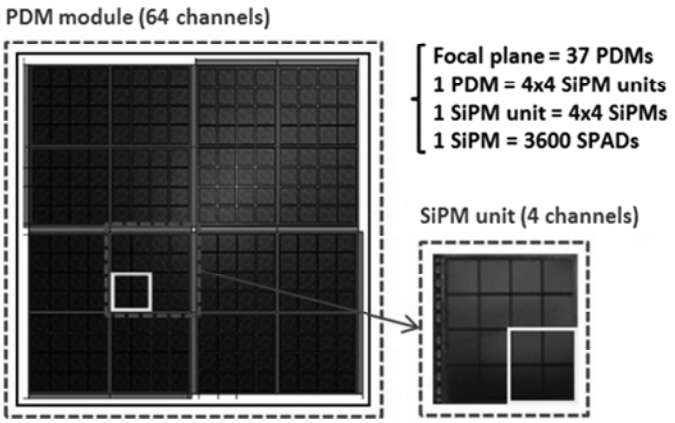

Figure 2. SiPM matrix pixels assembled into a PDM structural unit.

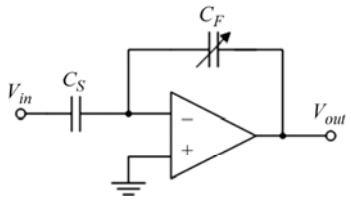

Figure 3. Schematic of the variable-gain operational amplifier embedded in the EASIROC chip.

4. Pre-amplifier Section Model

Each channel of the EASIROC chip embeds a pair of independently programmable variable-gain pre-amplifiers ensuring a versatile coverage of the dynamic range depending on the specific application purpose. Both low-gain and high-gain input pre-amplifiers can be adjusted by the back-end digital control circuitry (FPGA), allowing a negative gain range from -1 to -15 for the low-gain pre-amplifier, and from -10 to -150 for the high-gain pre-amplifier.

The simplified schematic of the variable-gain capacitive-feedback amplifier in the EASIROC chip is shown in Fig. 3.

The above circuit architecture is employed to generate both a low-gain and a high-gain closed-loop transfer function $A_V(s)$ by means of the tuneable feedback capacitance C_F.

The circuit models of the low-gain and high-gain pre-amplifier sections are implemented as illustrated in Fig. 4. The adjustable feedback capacitance is henceforth realized by exploiting a combination of parallel circuit branches including the series connection between a fixed-valued capacitor and a voltage-controlled switch.

As a consequence of the adopted connection, the resulting transfer function is strongly related to the amplitude of the DC voltage signal controlling the switches

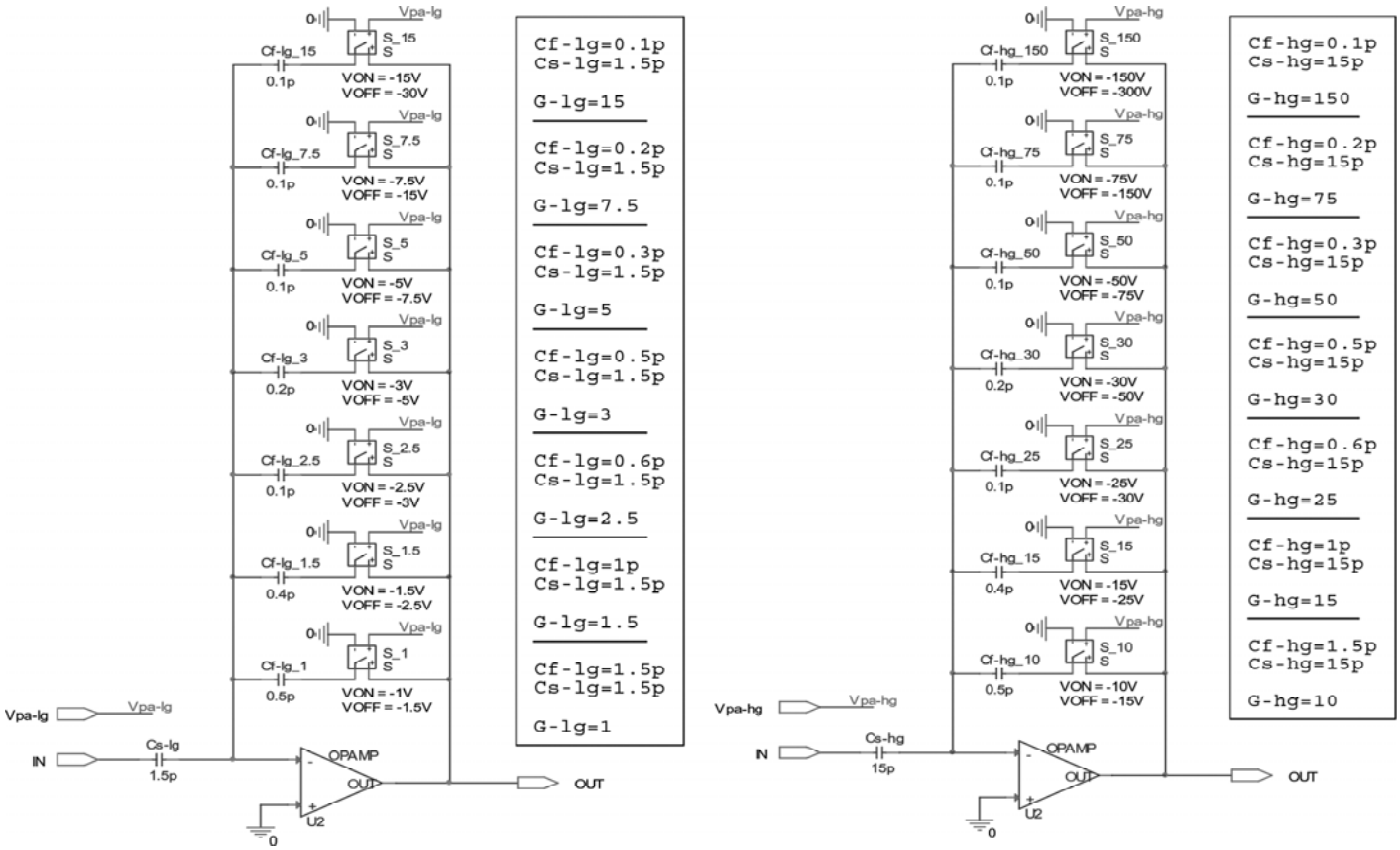

Figure 4. Schematic circuit model of the low-gain (on the left) and high-gain (on the right) pre-amplifier sections of the EASIROC chip.

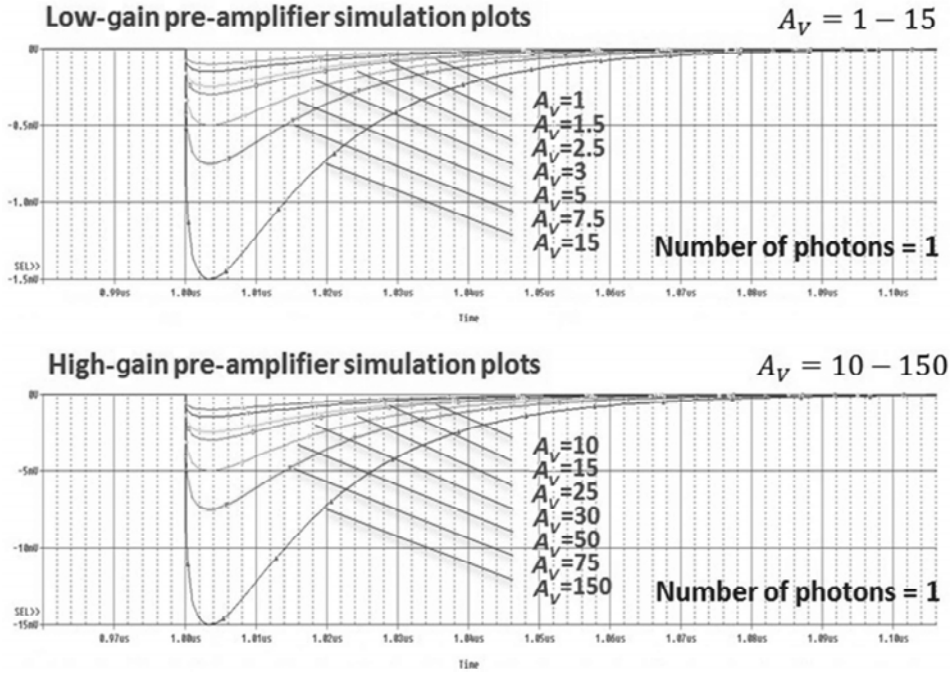

Figure 5. Simulated time responses of the low-gain (top) and high-gain (bottom) pre-amplifier models for all achievable gains and a single input photon.

and can be expressed as a function of the digital switch state

$$A_V(s) = -\frac{C_S}{\sum_i C_{Fi} S_i} \tag{1}$$

where C_{Fi} is the ith feedback branch capacitor and S_i is the logic value associated with the ith controlled switch S_i.

More specifically, referring, for instance, to the low-gain pre-amplifier model in Fig. 6, when the sole switch S_15 is closed, capacitor C_F_15 turns out to be the unique contribution to the overall feedback capacitance, and a voltage gain of -15 is obtained. Similarly, when the switch S_7.5 is in the on-state, the equivalent feedback capacitance is given by the parallel connection of C_F_15 and C_F_7.5, thus decrementing the resulting negative gain to -7.5. When all switches are turned on, the feedback loop capacitors in all branches are parallel-connected for an overall contribution of 1.5 pF, implying a minimum achievable gain of -1. Seven theoretical gain values can be accomplished for the adopted low-gain and high-gain pre-amplifier models, as also indicated in the right-side tables in Fig. 6.

Both tuneable signals controlling the feedback switches for the low-gain and high-gain pre-amplifiers are modelled by two DC voltage sources of adjustable values, whose labels are included in the list of PSICE parametric global variables. Therefore, in order to achieve a specific gain value for each input pre-amplifier, the user simply has to assign the corresponding DC voltage values to the global parameters {V_{pa}-lg} and {V_{pa}-hg}.

A parametric transient sweep analysis is carried out for both input pre-amplifiers by setting up all different voltage gains through the dedicated global variables and plotting the associated family curves. The time response of each pre-amplifier model to a single input pulse is illustrated in Fig. 5. The negative peak voltages of the output pulses are found to raise linearly with increasing values of the amplifier gain A_V for both low-gain and high-gain pre-amplifiers, thus confirming the accuracy of the adopted model.

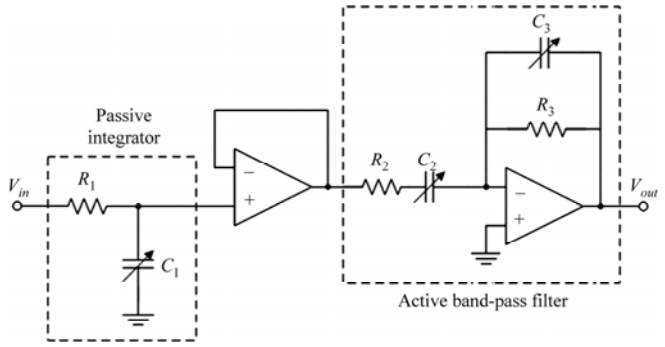

Figure 6. Schematic of the variable shaping time slow-shapers embedded in the EASIROC chip.

The amplified pulses at the output of the pre-amplifiers are then applied to the input of the noise-shaping filters.

5. Slow-Shaper Section Model

A slow noise-shaper section with selectable shaping time is integrated in each EASIROC channel to provide charge measurement. A dual-active slow-shaper chain is inserted at the output of both low-gain and high-gain pre-amplifiers.

The simplified schematic of the programmable shaping time slow-shapers of EASIROC is depicted in Fig. 6.

The above circuit topology is composed by a common passive RC integrator cascaded with an active band-pass filter. A unity-gain buffer is introduced between them to avoid loading effects. All time constants of the above circuit structure are designed to be identical by means of a suitable choice of the passive elements. Seven slow-shaping times can be selectively generated, ranging from 25 to 175 ns with a 25-ns linear increment.

Assuming ideal open-loop amplifiers for the slow-shaper circuit architecture in Fig. 9, the circuit small-signal transfer function is expressed by a third-order polynomial:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{sR_3C_2}{(1+sR_1C_1)(1+sR_2C_2)(1+sR_3C_3)} \tag{2}$$

Under the following design conditions on the passive elements:

$$R_1C_1 = R_2C_2 = R_3C_3 = \tau \tag{3}$$

The slow-shaper transfer function can be more conveniently rewritten as a function of the shaping time τ, thus yielding:

$$H(s) = -\frac{R_3}{R_2}\frac{s\tau}{(1+s\tau)^3} = -\frac{C_2}{C_3}\frac{s\tau}{(1+s\tau)^3} \tag{4}$$

The slow-shaper filter has a triple-pole transfer function, with a single zero at the origin of the complex s-plane generated by the series capacitor C_2. The pole frequency is determined by the reciprocal of the time constant in (3).

The magnitude of $H(s)$, calculated at the purely imaginary complex frequency $s = j\omega$, can be easily derived as:

$$|H(j\omega)| = \frac{R_3}{R_2}\frac{\omega\tau}{\sqrt{\left[1+(\omega\tau)^2\right]^3}} = \frac{C_2}{C_3}\frac{\omega\tau}{\sqrt{\left[1+(\omega\tau)^2\right]^3}} \tag{5}$$

By nullifying the first derivative in (5) with respect to the angular frequency ω yields the left half-plane pole frequency, ω_{peak}, at which the magnitude of the slow-shaper transfer function assumes the highest value:

$$\omega_{peak} = \frac{1}{\sqrt{2}\tau} \tag{6}$$

Substituting this peak frequency into the original slow-shaper transfer function expression in (4), the amplitude of the maximum obtainable gain is established:

$$|H(j\omega_{peak})| = \frac{4}{3\sqrt{3}} \cdot \left(\frac{1}{2}\frac{R_3}{R_2}\right) = \frac{4}{3\sqrt{3}} \cdot \left(\frac{1}{2}\frac{C_2}{C_3}\right) \tag{7}$$

Therefore, a maximum constant gain independent of the shaping time τ and related to a resistance or a capacitance ratio is achieved for the employed slow-shaper topology.

The circuit models of both low-gain and high-gain slow-shapers are implemented as shown in Fig. 7. Three circuit branches including parallel-connected capacitors and voltage-controlled switches are exploited to adjust the shaping time constant τ. In particular, the switching signals in each branch are synchronized to each other to control the three RC constants simultaneously. As a result, the tunable shaping time τ of the slow-shaper models can be expressed as:

$$\tau = R_1\sum_i C_{1i}\,S_{1i} = R_2\sum_i C_{2i}\,S_{2i} = R_3\sum_i C_{3i}\,S_{3i} \tag{8}$$

being C_{1i}, C_{2i} and C_{3i} the fixed capacitors in the ith branches, and S_{1i}, S_{2i} and S_{3i} the digital states of the ith switches.

More specifically, when only switches S_1_25n, S_2_25n and S_3_25n are on, capacitors C_1_25n, C_2_25n and C_3_25n turn out to be the unique contributions to the overall parallel capacitances, and the slowest time constant is set for all RC branches. Similarly, when switches S_1_50n, S_2_50n and S_3_50n also enter the on-state, the equivalent branch capacitances get raised accordingly, thus increasing the resulting shaping time. When all switches are turned on, all capacitors become parallel-connected, yielding the slowest time constant value in all three branches. Seven theoretical shaping times can be accomplished for the adopted low-gain and high-gain slow-shaper models, as tabulated in Fig. 7. To this aim, the off-state thresholds deactivating the switches are properly synchronized to avoid undesired overlap.

The tuneable signal controlling the slow-shaper switches is realized through an adjustable DC voltage source, whose absolute value can be selected by the parametric global variable $\{V_{sh}\}$ defining the shaping time constant.

Parametric frequency and transient sweep analyses are performed on the implemented slow-shaper model by varying the shaping time constant as well as the number of input pulses. To get the time constants ranging from 25 to 175 ns with the capacitor values listed in Fig. 7, resistors R_1, R_2 and R_3 of both EASIROC low-gain and high-gain slow-shapers are chosen to be 20, 50 and 200 kΩ, respectively.

To evaluate the spectral response of the proposed slow-shaper model and validate the frequency analysis, AC magnitude simulations are carried out as functions of the tuneable shaping times. Parametric sweep results for all available values of the slow-shaper time constant are shown in Fig. 8 in linear and logarithmic scales.

As expected by the theoretical pencil-and-paper evaluation, all spectral curves linearly rise up with a positive 20-dB per-decade excursion until the third-order pole frequency, and afterwards decrease by a negative 40-dB per decade linear slope. The system cut-off frequency is inversely proportional to the shaping time constant, in agreement with (6), hence ranging between 640 kHz (for $\tau = 175$ ns) and 4.5 MHz (for $\tau = 25$ ns). On the other side, the magnitude of the peak frequency is independent of the specific shaping time, and reaches a maximum value of 3.85 in accordance with (7).

To confirm the effectiveness of the adopted model, parametric transient sweeps are performed as well. Figure 9

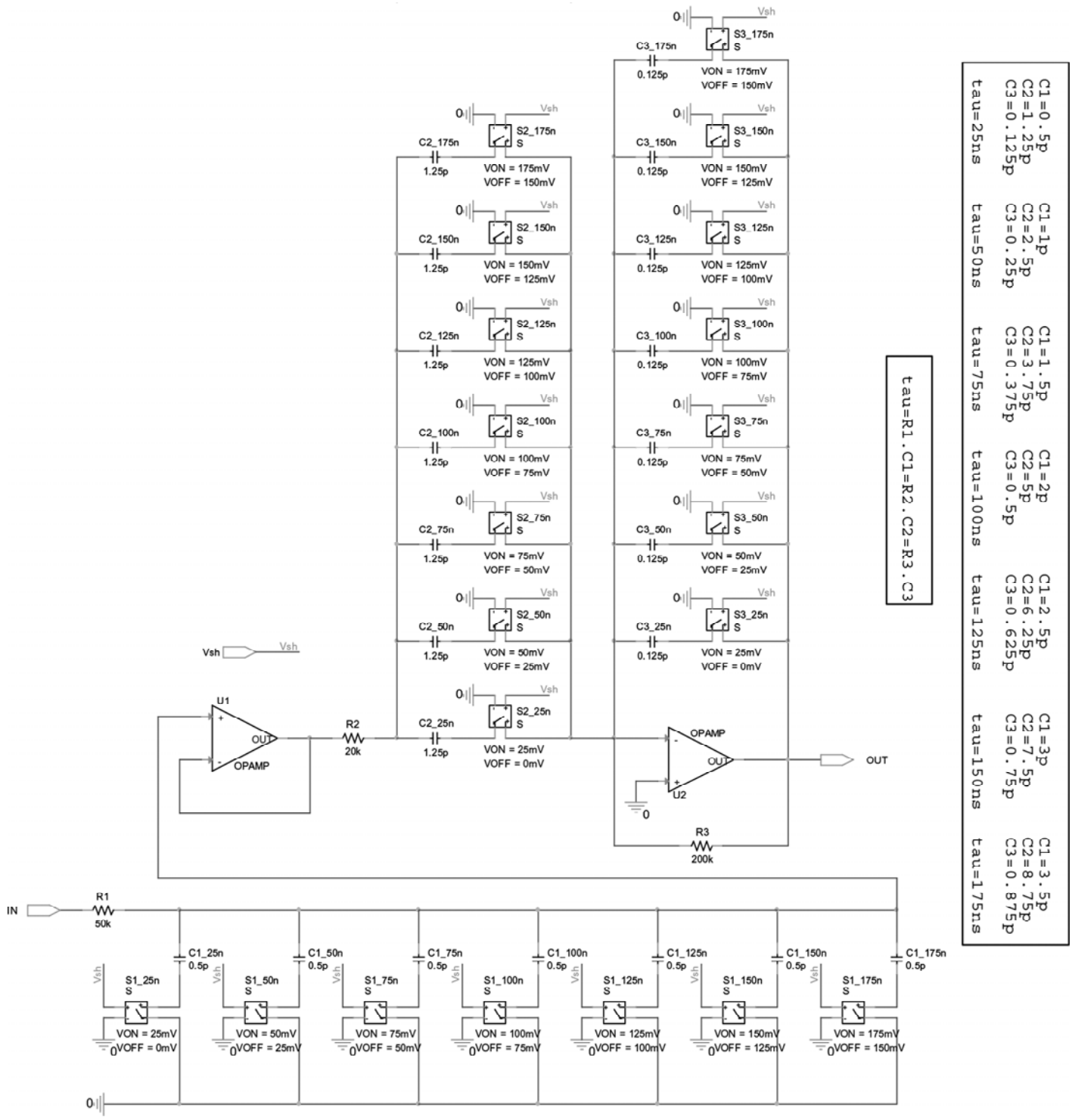

Figure 7. Schematic circuit model of the tuneable shaping time slow-shapers of the EASIROC chip (on the left) and tuneable capacitor values and relevant shaping times for the adopted slow-shaper model (on the right).

depicts the time-domain response of both slow-shapers to an input photon pulse and turns out to be particularly helpful to evaluate the correlation between the slow-shaper time constant and the peaking time of its transient response.

Observing the curve plots, it can be inferred that greater shaping time values produce the effect of modulating the slow-shaper output waveform by decreasing its peak amplitude and delaying its peaking time.

Parametric simulations of the slow-shaper transient responses to different input voltage pulses, for a fixed shaping time, show that the amplitude of the slow-shapers linearly grows with increasing values of the input peak voltage, but the peaking times of the shapers are found to

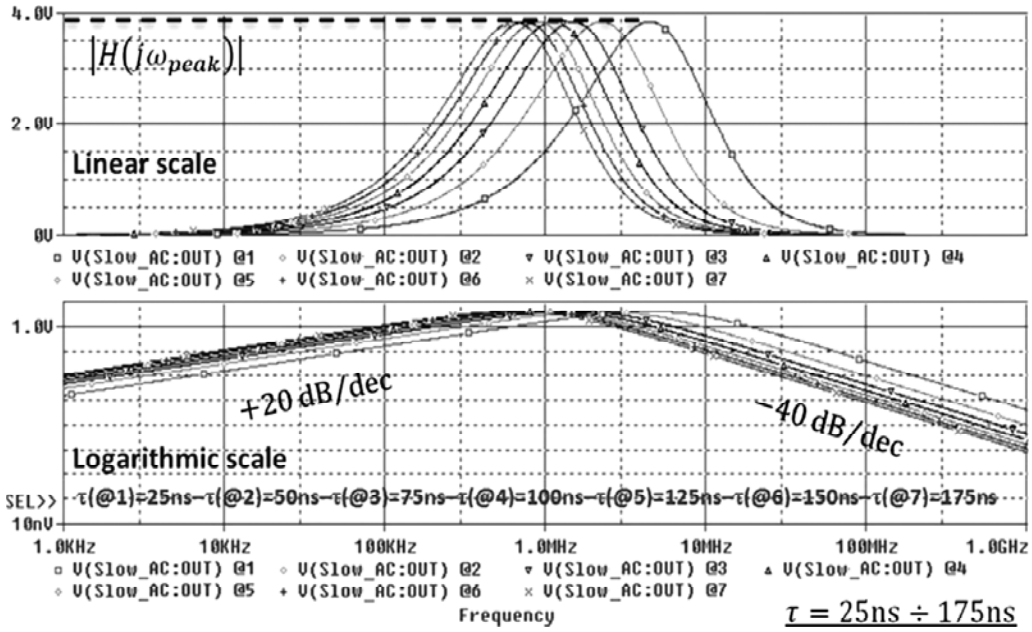

Figure 8. Linear (on top) and logarithmic (on bottom) frequency responses of the slow-shaper circuit.

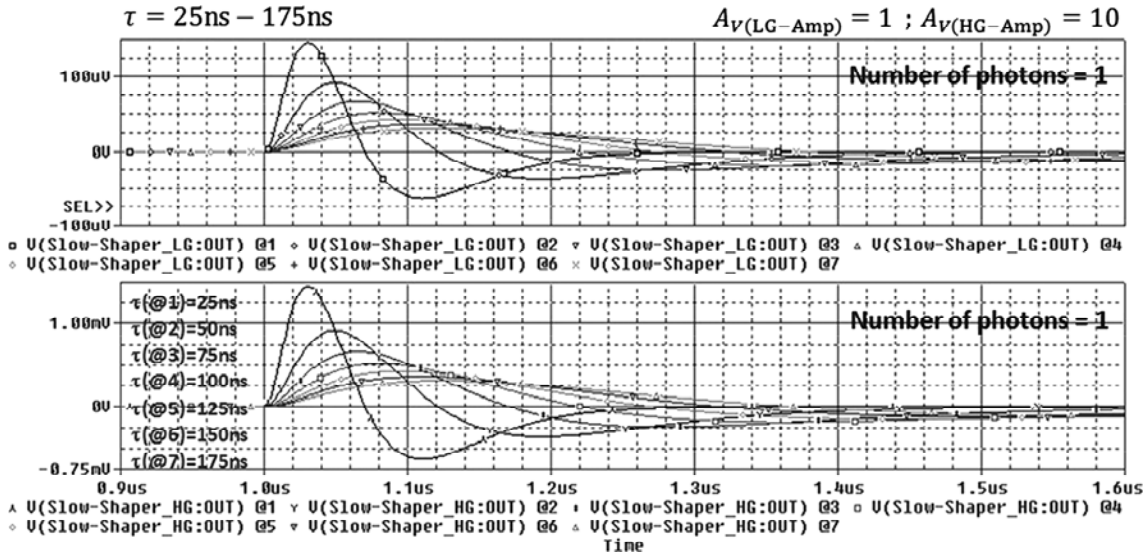

Figure 9. Parametric transient responses of the low-gain and high-gain slow-shaper circuit models to a single input photon pulse under a minimum pre-amplifier gain, for all available shaping time values.

have the same values regardless of the number of photons detected.

The low-gain and high-gain slow-shaper signals finally get to the sample-and-hold sections of the front-end model, which memorize the analogue values of the shaped signals when approaching their peak voltage.

6. Trigger Generation Model

EASIROC also features a fast-shaper section with a fixed shaping time, following the high-gain pre-amplifier. The output signal is then compared to a selectable threshold by means of a line discriminator, providing the trigger signal.

The simplified schematic of the EASIROC fast-shaper is depicted in Fig. 10.

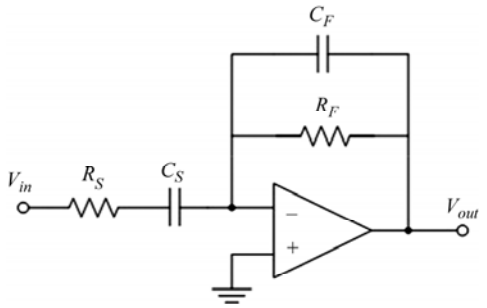

Figure 10. Schematic of the fast-shaper circuit embedded in the EASIROC chip.

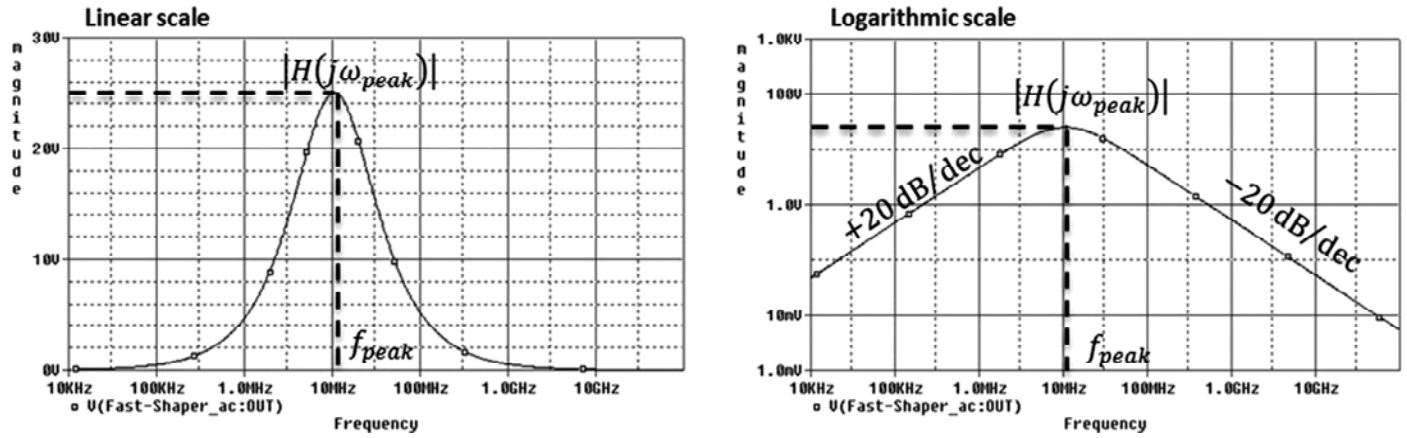

Figure 11. Linear (on the left) and logarithmic (on the right) frequency responses of the fast-shaper circuit.

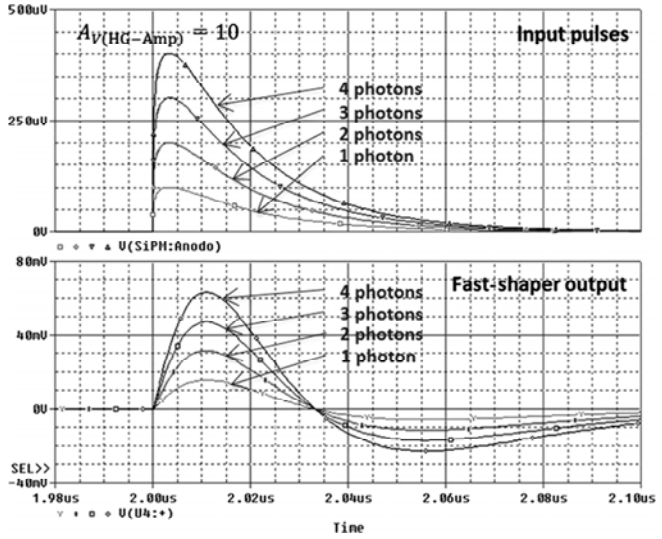

Figure 12. Parametric transient responses of the fast-shaper model under a minimum pre-amplifier gain.

Assuming an ideal open-loop amplifier, the circuit small-signal transfer function is expressed by:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{sR_FC_S}{(1+sR_SC_S)(1+sR_FC_F)} \tag{9}$$

Under the following design conditions on the passive elements:

$$R_SC_S = R_FC_F = \tau \tag{10}$$

The above fast-shaper transfer function can be expressed as a function of the shaping time constant τ, hence yielding

$$H(s) = -\frac{R_F}{R_S}\frac{s\tau}{(1+s\tau)^2} = -\frac{C_S}{C_F}\frac{s\tau}{(1+s\tau)^2} \tag{11}$$

The fast-shaper filter has a second-pole transfer function, with a single zero at the origin of the complex s-plane generated by the series capacitor C_S. The frequency of the second-order multiplicity pole is determined by the reciprocal of the time constant τ, as occurs in the slow-shaper transfer function.

The magnitude of the transfer function $H(s)$, calculated at the purely imaginary complex frequency $s = j\omega$, is:

$$|H(j\omega)| = \frac{R_F}{R_S}\frac{\omega\tau}{1+(\omega\tau)^2} = \frac{C_S}{C_F}\frac{\omega\tau}{1+(\omega\tau)^2} \tag{12}$$

By nullifying the first derivative of (13) with respect to the angular frequency yields the left half-plane pole frequency, ω_{peak}, at which the magnitude of the slow-shaper transfer function assumes the highest value:

$$\omega_{peak} = \frac{1}{\tau} \tag{13}$$

Substituting (13) into the fast-shaper transfer function in (11), the amplitude of the maximum gain is obtained:

$$|H(j\omega_{peak})| = \frac{1}{2}\frac{R_F}{R_S} = \frac{1}{2}\frac{C_S}{C_F} \tag{14}$$

Therefore, as for the slow-shaper circuits, a maximum constant gain independent of the shaping time and related to a resistance or a capacitance ratio is achieved for the employed fast-shaper topology.

Parametric frequency and transient sweep analyses are performed on the implemented fast-shaper model by varying the number of input photon pulses. To achieve a 15-ns fast-shaping constant, resistors R_S and R_F are chosen to be 1.5 and 75 kΩ, respectively, whilst capacitors C_S and C_F are designed to be 10 pF and 200 fF, respectively.

To evaluate the frequency response of the fast-shaper model and verify the developed analysis, AC magnitude simulations are carried out in both linear and logarithmic scale, as illustrated in the relevant graphs in Fig. 11.

As expected by the theoretical evaluation, the spectral curve increases by 20 dB per decade until the second-order pole frequency, and afterwards decreases by 20 dB per decade. The system cut-off frequency is found to be 11 MHz, in agreement with (13). The magnitude at this

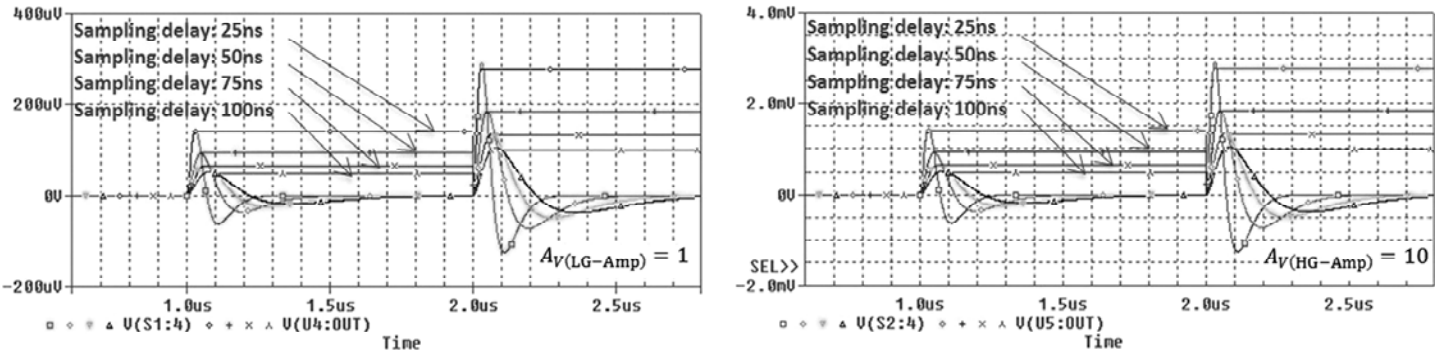

Figure 13. Transient simulation results of the track-and-hold cells outputs for different values of the sampling times from the pulse rise.

frequency reaches a maximum value of 25, in accordance with (14).

To validate the effectiveness of the adopted model when processing the voltage pulses coming from the high-gain pre-amplifier section of the SiPM front-end, parametric transient sweeps are also performed. Figure 12 depicts the time-domain response of the fast-shaper to different incident photon pulses, for the minimum pre-amplifier high gain.

The amplitude of the fast-shaper output waveform linearly grows with increasing peak values of the input pulse voltage. An overall gain factor of about 16 is detected for the adopted fast-shaper model with respect to the input pulse.

Once again, the correlation between the shaping constant and the peaking time of the fast-shaper time response is evident. An 11.2-ns delay time is found from the raising of the input pulses, regardless of their voltage amplitudes.

The voltage output from the fast-shaping channel is then compared to an adjustable threshold discriminator cascaded with the fast-shaper circuit, as shown in the schematic model of Fig. 1, in order to generate a trigger signal.

The adjustable threshold of the discriminator is modelled by a voltage generator with a tuneable DC value, whose label, $\{V_{th}\}$, is added to the list of PSPICE parametric global variables.

7. Sample-and-Hold Section Model

The EASIROC analogue front-end is expected to control and save the amplitude of the shaped signal when approaching its peak value. This is accomplished by two analogue track-and-hold cells at the end of the dual-line chain.

The schematic circuit model of the implemented analogue memory for the digital acquisition of the peak amplitude information is shown in Fig. 1 for both shaping lines of the EASIROC channel. A voltage-controlled switch is exploited to regulate the sampling frequency of the memory cells, a storage capacitor C is adopted to supply the dynamic storage of the analogue data, and a unitary-gain amplifier is finally connected at the output of each memory cell to maintain a correct analogue information and prevent the voltage stored on the capacitor from decaying.

The value of the storage capacitor has to be accurately chosen, in a design step, to fulfil a suitable trade-off between contradicting design requirements. In fact, an excessively small-valued C would entail some unavoidable voltage losses of the stored information, due to the finite equivalent impedance of the controlled switches; conversely, too high values of C would involve a remarkable exponential rise time delay when sampling the analogue voltages coming from the slow-shaper outputs. For the realized model design an optimum capacitor value of 100 pF is determined.

The voltage pulse generator V_{hold} is used to sense the controlled switches according to the desired sampling frequency. For the actual design, based on the existing connection between the shaping constant of the slow-shaper circuits and the peaking time of their shaped output waveforms, the sampling clock is chosen as to have a pulse-width (from the input pulse rise) equal to the preceding slow-shaper time constant. To this aim, the global variable $\{V_{sh}\}$, controlling the shaping time of the low-gain and high-gain shapers, is also added to the pulse-width field of the voltage source V_{hold}.

The simulated output waveforms of the track-and-hold cells, for different shaping time values and two input pulses, are reported in Fig. 13. The pulse-width value of V_{hold}, controlling the switching frequency, is synchronized with the nominal shaping time of the high-gain slow-shaper by means of the same parametric variable definition. So, the analogue value of the shaped signal is stored across capacitor C after a time delay given by the slow-shapers time constant.

Read-out operation of these analogue memory cells is then performed by the digital registers of the back-end FPGA.

8. Conclusion

The fully analogue EASIROC front-end model for the SiPM signal read-out is analysed and developed. A particular emphasis is devoted not only to the

purely theoretical aspects, but also to a powerful design approach. PSPICE simulations of each single section model are performed to validate the implemented front-end. Transient and frequency responses for each circuit block are carried out to illustrate the circuit model behaviour and confirm the analytical design equations. The proposed front-end model provides a useful simulation tool for analysing the operating principle and evaluating possible deviations of the actual response of the EASIROC electronics from the analytical approach used.

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Biographies

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Salvatore Garozzo was born in Catania, Italy, in 1978. He received the M.Sc. degree in Electronic Engineering in 2004 from the University of Catania, upon discussing a dissertation on AMOLED display drivers, performed at ST-Microelectronics in Catania. In 2010, he has worked as a construction supervisor in a company of electrical systems. Since 2006 he has been serving as a professor of electronics at secondary high school. Since 2012 he has been working at the Osservatorio Astrofisico di Catania (OACT), within the Istituto Nazionale di Astrofisica (INAF), as a junior design engineer. His main research activities include the analysis and design of analog and mixed-signal integrated circuits He is involved in the electronic design of high-performance integrated circuits and custom electronics based on field programmable gate array (FPGA).

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